REMARKS

Claims 1, 3-4 and 16-23 are all the claims presently being examined in the application. Applicant has canceled Claim 2 without prejudice or disclaimer. Claims 5-15 were previously canceled without prejudice or disclaimer. Claims 1, 3-4 and 16-23 stand rejected on prior art grounds.

With respect to the prior art rejections, claims 1, 3, and 21 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over the acknowledged prior art of Fig. 1 in view of Takenaka, et al. (U.S. Patent No. 5,278,429). Claims 2 and 16 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over the acknowledgment prior art of Fig. 1 in view of Takenaka, et al., and further in view of Enomoto, et al. (U.S. Patent No. 5,055,321). Claim 17 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over the acknowledged prior art of Fig. 1 in view of Takenaka, et al. and further in view of Kaskoun, et al. (U.S. Patent No. 5,816,478). Claims 4, 18, 19, and 22 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Kweon, et al. (U.S. Patent No. 5,834,832) in view of Takada, et al. (U.S. Patent No. 6,344,753). Claims 20 and 23 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over the acknowledged prior art of Fig. 1 in view of Hashimoto (U.S. Patent No. 6,323,542).

These rejections are respectfully traversed in view of the following discussion.

Entry of this 1.116 Amendment is proper. Since the amendments above narrow the issues for appeal and since such features were in the claims earlier, such amendments do not raise a new issue requiring further searching and/or consideration by the Examiner. As such entry of this Amendment is believed to be proper and is earnestly solicited.

It is noted that the amendments are made only to more particularly define the invention and not for distinguishing the invention over the prior art, for narrowing the scope

of the claims, or for any reason related to a statutory requirement for patentability.

It is further noted that, notwithstanding any claim amendments made herein, Applicant's intent is to encompass equivalents of all claim elements, even if amended herein or later during prosecution.

I. THE CLAIMED INVENTION

Applicant's invention, as disclosed and claimed, for example by independent claim 1, is directed to a semiconductor device.

The semiconductor device includes a semiconductor chip, a chip-mounting substrate which is provided with the semiconductor chip mounted on a top surface thereof and first conductive pads formed on a bottom surface thereof and connected with the semiconductor chip electrically, solder balls formed on the first conductive pads, a printed circuit board on which second conductive pads connected with the solder balls are formed, and a solder mask formed on a bottom surface of the chip-mounting substrate. The solder mask includes a first uneven roughness, and underfill material is injected into a clearance formed between the chip-mounting substrate and the printed circuit board. The first uneven roughness is formed on a surface which is brought into contact with the underfill material. The first uneven roughness increases an area of a contact surface between the chip-mounting substrate and the underfill material. Importantly, at least one of the first conductive pads and the second conductive pads includes a second uneven roughness. (See Page 17, lines 23-25; Page 19, lines 1-4 and 15-24; and Page 20, lines 6-9; and Figures 5-6).

Independent claim 4, is also directed to a semiconductor device. The semiconductor device includes a semiconductor chip, a lead frame which is provided with the semiconductor chip mounted thereon and electrically connected with the semiconductor chip, and a printed

circuit board including conductive pads which are formed thereon and brought into direct contact with a bottom surface of the lead frame. The uneven roughness exists on the bottom surface of the lead frame and a surface of the conductive pads. (See Page 20, lines 10-25; and Page 21, lines 18-28; Page 22, lines 6-11; and Figures 9A and 9B).

Independent claim 20, is also directed to a semiconductor device. The semiconductor device includes a semiconductor chip, a chip-mounting substrate which is provided with the semiconductor chip mounted on a top surface thereof and first conductive pads formed on a bottom surface thereof and connected with the semiconductor chip electrically, the chip-mounting substrate including Cu wirings, solder balls formed on the first conductive pads, a printed circuit board on which second conductive pads connected with the solder balls are formed, and material injected into a clearance formed between the chip-mounting substrate and the printed circuit board. A first uneven roughness is formed on a contact surface between the Cu wirings of the chip-mounting substrate and the solder balls. The first uneven roughness exists on a bottom surface of the Cu wirings, and the Cu wirings are directly connected to the solder balls to form a joined surface. Importantly, the second conductive pad includes a second uneven roughness portion in contact with the solder balls. (See Page 17, lines 23-25; Page 19, lines 1-4 and 15-24; and Page 20, lines 6-9; and Figures 5-6).

Conventional semiconductor devices do not have an uneven roughness formed on a bottom surface of a chip-mounting substrate, a pad situated between the solder ball and the insulating substrate or a pad on a printed circuit board. This conventional configuration tends to decrease reliability because a reduction occurs in the adhesive strength of an underfill material due to contamination or external mechanical stresses thus causing the underfill material to exfoliate from the chip-mounting substrate or the printed circuit board. (See Page 1, line 22 - Page 2, line 24; and Figure 1).

An aspect of the present invention includes that at least one of the first conductive pads and the second conductive pads includes a second uneven roughness. This configuration through the use of the solder mask "seals the lands and the Cu wirings airtightly and the surfaces thereof can be made rough easily," which promotes greater adhesive strength among the chip-mounting substrate, the underfill material and the printed circuit board (according to claim 1). (See Page 4, line 17 through Page 5, line 4; Page 17, lines 23-25; Page 19, lines 1-4 and 15-24; and Page 20, lines 6-9; and Figures 5-6). .

A similar feature in a semiconductor device, as disclosed and claimed, for example by independent claim 4, includes an uneven roughness existing on a bottom surface of the lead frame and the surface of the conductive pads, which provides greater adhesive strength between the lead frame and the printed circuit board. (See Page 20, lines 10-25; and Page 21, lines 18-28; Page 22, lines 6-18; and Figures 9A and 9B).

A similar feature in a semiconductor device, as disclosed and claimed, for example by independent claim 20, includes the first uneven roughness existing on a bottom surface of the Cu wirings with the Cu wirings being directly connected to the solder balls to form a joined surface, which provides greater adhesive strength between the Cu wirings and the solder balls. (See Page 19, lines 1-4; and lines 15-24; Page 20, lines 10-25; and Page 21, lines 18-28; and Figures 5 and 6).

As a result of these features, the semiconductor device experiences less internal exfoliation of the components, and thus operates with a high level of reliability. (See Page 3, lines 15-21; Page 19, lines 22-24; and Page 22, lines 17-18).

II. THE PRIOR ART REJECTION

A. The § 103(a) Rejection of the Acknowledged Prior Art in view of Takenaka, et al.

Regarding claims 1, 3 and 21, first, the references, separately, or in combination, fail to teach, disclose or provide a motivation for being combined.

In particular, the Prior Art discloses a semiconductor device, which includes a printed circuit board and a semiconductor chip mounting substrate with an underfill material, and is specifically directed to solving a problem of the different thermal expansion coefficients between the printed circuit board and the chip mounting substrate by providing for an underfill material to absorb a stress caused by these expansions. (See Page 1, line 22- Page 2, line 25). However, the Prior Art devices have decreased reliability because a reduction occurs in the adhesive strength of an underfill material due to contamination or external mechanical stresses thus causing the underfill material to exfoliate from the chip-mounting substrate or the printed circuit board. (See Page 1, line 22 - Page 2, line 24; and Figure 1).

By contrast, Takenaka, et al. ("Takenaka") does not have the same aim as the Prior Art.

Takenaka discloses a semiconductor device having an improved adhesive structure, and related method. Takenaka is specifically directed to improving the adhesion between a package, which accommodates a semiconductor chip, and a cover over the package through an adhesive portion with increased adhesion strength. (See Takenaka at Abstract; Column 1, lines 10-25; and Column 2, lines 5-20).

Nothing within Takenaka, which focuses on improving adhesive strength between the package and the cover of a semiconductor, has anything to do with underfill material for differences in thermal coefficients of expansion with potentially reduced adhesive strength as

disclosed in the Prior Art. Thus, the Prior Art teaches away from being combined with another invention, such as, Takenaka.

Therefore, one of ordinary skill in the art would not have combined these references, absent hindsight.

Second, even if combined, the references do not teach or suggest the features of independent claim 1, including at least one of the first conductive pads and the second conductive pads including a second uneven roughness. (See Page 17, lines 23-25; Page 19, lines 1-4 and 15-24; and Page 20, lines 6-9; and Figures 5-6).

The Prior Art, as discussed above, pertains to semiconductor chips, which are attached to printed circuit boards, without an uneven roughness existing on a bottom surface of a chip-mounting substrate or a pad situated between the solder ball and the insulating substrate. Indeed, the Prior Art does not disclose, teach or suggest improving surface bonding. (See Column 2, lines 39-48; and Page 2, line 25 through Page 3, line 21). Accordingly, Applicant agrees with the assertion in the Office Action that the Prior Art is deficient, and thus "does not disclose a solder mask formed on a bottom surface of the chip-mounting substrate, ..." (See Office Action, Page 3-4, Section 5).

Takenaka does not make up for the deficiencies of the Prior Art.

Instead, Figures 12 and 14 of Takenaka discloses a package 21 with a solder resist layer 85 on top of a portion of the package 21, an alumina paste layer 45 on top of the solder resist layer 85, a semiconductor chip 12 mounted on top of the alumina paste layer or an additional silver glass layer, and a lid on top of the semiconductor chip. The solder resist layer "is coated on the package by the screen printing process" and has a surface roughness. (See Column 8, lines 52-61; Column 9, lines 55-67; and Figures 12 and 14). Thus, contrary to the assertion in the Office Action, Takenaka only teaches that the solder resist layer 85 is

formed on the package 21 without any solder balls, let alone, solder balls formed on first and second conductive pads as taught by Applicant's invention.

In contrast to Takenaka, Applicant's invention discloses that at least one of the first conductive pads and the second conductive pads includes a second uneven roughness. In particular, "solder balls are connected with the Cu wirings by thermal compression, where the surface of the Cu wirings have been made roughened before hand." "[S]ince areas of jointed surfaces between the Cu wirings (the pads) and the solder balls increase because of unevennesses provided for the surfaces of the Cu wirings (the pads), the adhesive strength between the Cu wirings and the solder balls are heightened." Further, "[a]lthough unevennesses are provided for the pads formed on the chip-mounting substrate in the aforementioned embodiment, unevennesses may [be] provided for the pads formed on the printed circuit board as shown in FIG. 6A. Morever, as shown in FIG. 6B, unevennesses may be provided for the pads respectively formed on the chip-mounting substrate and the printed circuit board." (See Page 19, lines 1-20; and Page 20, lines 3-10).

As indicated, Takenaka does not disclose or suggest any type of solder balls or conductive pads, let alone, at least one of the first conductive pads and the second conductive pads selectively including a second uneven roughness.

Indeed, Takenaka forms the solder resist layer directly on the package, not on a pad situated on a printed circuit board nor at the interface between the Cu wiring (pad) and a solder ball to achieve the advantages of Applicant's invention.

Therefore, neither the Prior Art nor Takenaka discloses, teaches or suggests, that at least one of the first conductive pads and the second conductive pads includes a second uneven roughness as recited in claim 1.

For at least the reasons outlined above, Applicant respectfully submits that neither the

Prior Art nor Takenaka discloses, teaches or suggests all of the features of the independent claim 1, and related dependent claims 3 and 21, which are patentable not only by virtue of their dependency from the respective independent claim 1, but also by the additional limitations they recite.

B. The Enomoto Reference

Regarding claim 2, which has been incorporated into claim 1, and similarly claim 16, to make up for the deficiencies of the Prior Art and Takenaka as discussed above, the Examiner relies on Enomoto, et al. ("Enomoto"). Enomoto fails to do so.

First, Enomoto does not have the same aim as either the Prior Art or Takenaka as discussed above, and the urged combination would not have been made, absent hindsight.

Enomoto's discloses an adhesive for electroless plating formed by dispersion of heat-resistant granules soluble in a heat resistant resin. (See Enomoto at Abstract). Enomoto is specifically directed to solving the drawbacks in the adhesive for electroless plating in producing the printed circuit boards (PCBs). Indeed, Enomoto attempts to increase the adhesion property between a PCB and the patterns thereon. (See Column 1, lines 5-15; and Column 2, lines 38-48).

Nothing within Enomoto, which focuses on adhesives for electroless plating, has anything to do with underfill material for differences in thermal coefficients of expansion as disclosed in the Prior Art. Thus, the Prior Art teaches away from being combined with another invention, such as, Enomoto.

Similarly, nothing within Enomoto has anything to do with improving adhesive strength between the package and the cover of a semiconductor as disclosed in Takenaka. Thus, the Prior Art and Takenaka teach away from being combined with each other as well

another invention, such as, Enomoto.

Therefore, one of ordinary skill in the art would not have combined these references, absent hindsight.

Secondly, Enomoto does not disclose, teach or suggest including at least one of the first conductive pads and the second conductive pads includes a second uneven roughness as recited in claim 1.

Further, Enomoto does not disclose, teach or suggest, including the printed circuit board has a dimple-like shaped configuration as recited in claim 16.

Instead, Figure 1d of Enomoto teaches an adhesive for electroless plating formed by dispersion of heat-resistant granules soluble in a heat resistant resin. In particular, the surface of the interlaminar resin insulating layer is roughened, however, the circuit layer, for exemplary purposes only element 6, is not taught as bring roughened.

Contrary to the assertion in the Office Action, Applicant notes that the circuit layer is part of four layers used to form a multi-layer printed circuit board and is not a conductive pad, an element of Applicant's invention, as suggested in the Office Action (See Enomoto at Abstract; Column 9, lines 5-15; Column 10, lines 5-15 and 44-47; Figure 1; and Office Action, Page 5, 1st Paragraph). Since Enomoto does not disclose, teach or suggest "at least one of the first conductive pads and the second conductive pads selectively including a second uneven roughness," Enomoto is deficient and thus does not teach the specific limitations of dependent claim 16.

For the reasons stated above, the claimed invention, defined by independent claim 1, which incorporated dependent claim 2, and, separately, dependent claim 16, is fully patentable over the cited references.

C. The Kaskoun Reference

Regarding claim 17, to make up for the deficiencies of the Prior Art and Takenaka, the Examiner relies on Kaskoun, et al. ("Kaskoun"). Kaskoun fails to do so.

First, Kaskoun discloses a method of flip-chip bonding of two electronic components without the use of a flux material. (See Kaskoun at Abstract).

Kaskoun is specifically directed to solving the drawbacks in the soldering process of semiconductor device in assembling at least two electronic components. Indeed, Kaskoun attempts to eliminate "the risks of deforming the solder balls, and does not add appreciable complexity or cost to the manufacturing process." (See Column 1, lines 5-20 and 50-63; and Column 2, lines 29-57).

Nothing within Kaskoun, which focuses on flip-chip bonding without the use of a flux material, has anything to do with underfill material for differences in thermal coefficients of expansion as disclosed in the Prior Art. Thus, the Prior Art teaches away from being combined with another invention, such as, Kaskoun.

Similarly, nothing within Kaskoun has anything to do with improving adhesive strength between the package and the cover of a semiconductor as disclosed in Takenaka. Thus, the Prior Art and Takenaka teach away from being combined with each other as well another invention, such as, Kaskoun.

Therefore, one of ordinary skill in the art would not have combined these references, absent hindsight.

Secondly, Kaskoun does not disclose, teach or suggest including at least one of the first conductive pads and the second conductive pads includes a second uneven roughness as recited in claim 1.

Further, Kaskoun does not disclose, teach or suggest a chip-mounting substrate having

a slit-like shaped configuration as recited in claim 17.

Instead, Kaskoun discloses a method of flip-chip bonding without the use of a flux material. (See Kaskoun at Abstract; and Figure 1). Since Kaskoun do not disclose, teach or suggest "at least one of the first conductive pads and the second conductive pads selectively including a second uneven roughness," Kaskoun is deficient and thus does not teach the specific limitations of dependent claim 17.

For the reasons stated above, dependent claim 17 is fully patentable over the cited references.

D. The § 103(a) Rejection of Kweon, et al. in view of Takada, et al.

Regarding the rejection of claims 4, 18, 19 and 22, first, the references, separately, or in combination, fail to teach, disclose or provide a motivation for being combined.

Kweon, et al. ("Kweon") pertains to a packaging structure for a surface mounting type semiconductor package, specifically directed to "improving the grounding property by the particular packaging structure, which allows a reduction of the noise, without deteriorating the operation speed or mounting density of the package" by providing "a nonconductive thin film as a capacitor formed in a space between the die pad and the conductive pattern where the space has a voltage difference." (See Kweon at Abstract; Column 1, lines 10-23; and Column 3, lines 8-33).

By contrast, Takada, et al. ("Takada") does not have the same aim as Takada.

Takada discloses a test socket with improved contact terminals for measuring the electric characteristics of an electronic device. Takada is specifically directed to "ensure stable contact between the external terminals of an electronic device and contact terminals of a test socket, thus realizing stable, continuous contact." (See Takada at Abstract; Column 1, lines 5-15; Column 2, lines 35-45).

Nothing within Takada, which focuses on ensuring stable and continuous contact between the external terminals of an electronic device and contact terminals of a test socket has anything to do with "improving the grounding property by the particular packaging structure" as disclosed in Kweon. Thus, the Kweon teaches away from being combined with another invention, such as, Takada.

Therefore, one of ordinary skill in the art would not have combined these references, absent hindsight.

Second, even if combined, the references do not teach or suggest the features of independent claim 4, including that a printed circuit board including conductive pads which are formed thereon and brought into direct contact with a bottom surface of the lead frame, and an uneven roughness existing on the bottom surface of the lead frame and the surface of the conductive pads. (See Page 20, lines 10-25; and Page 21, lines 18-28; Page 22, lines 6-11; and Figures 9A and 9B).

Applicant agrees with the assertion in the Office Action that Kweon does not "disclose the unevenroughness existing on the bottom surface of the lead frame and a surface of the conductive pads." (See Office Action, Page 6, Section 8).

Takada does not make up for the deficiencies of Kweon. Instead, Figures 3A, 3B and 3C, of Takada disclose a conventional test socket with contact terminals. Applicant respectfully submits that the Office Action mischaracterizes Takada because the protruberances 22 and the recesses 23 are in contact with an external connection terminal 50 not a lead frame as asserted in the Office Action. (See Office Action, Page 6, Section 8). The external connection terminal 50, which appears to extend from a lead frame, includes an outermost solder plating film 55. An oxide film 56 is formed on the surface of the outermost layer (solder plating film) 55. In addition, the contact terminal 20 includes a contact

projection 24 with protrusions 22 and recesses 23 in the contact projection 24. Figure 3B clearly shows that the projections "fracture the oxide film of the external connection terminal and engage with the outermost layer (solder plating)" but not the underlying lead frame. Accordingly, an uneven roughness does not exist on the bottom surface of the lead frame and a surface of the conductive pads. (See Takada at Abstract; Column 4, line 17-Column 5, line 10; Column 6, lines 30-40) Contrary to the assertion in the Office Action, Takada only teaches that a surface roughness exists on the contact projection, not the bottom surface of the lead frame as recited in claim 4.

In contrast, Applicant's invention includes a printed circuit board including conductive pads which are formed thereon and brought into direct contact with a bottom surface of the lead frame, and an uneven roughness exists on the bottom surface of the lead frame and the surface of the conductive pads. Since the unevenroughness is formed on the lead frame and the conductive pads, this configuration provides for greater adhesive strength between the lead frame and the printed circuit board. (See Page 20, lines 10-25; and Page 21, lines 18-28; Page 22, lines 6-18; and Figures 9A and 9B).

As indicated, Takada only, at best, forms the roughness on the contact projection whereas in Applicant's invention the uneven roughness exists on the bottom surface of the lead frame and the surface of the conductive pads where the printed circuit board includes the conductive pads. As a result, the Takada configuration may result in reduced adhesion between the lead frame and the printed circuit board when compared to Applicant's invention.

Therefore, neither Kweon nor Takada teaches or suggests a printed circuit board including conductive pads which are formed thereon and brought into direct contact with a bottom surface of the lead frame, and an uneven roughness exists on the bottom surface of the

lead frame and the surface of the conductive pad as recited in independent claim 4. Thus, the invention provides for greater adhesive strength between the lead frame and the printed circuit board, and thus the semiconductor device experiences less internal exfoliation of the components and operates with a high level of reliability. (See Page 3, lines 15-21; Page 20, lines 10-25; and Page 21, lines 18-28; Page 22, lines 6-18; and Figures 9A and 9B).

For at least the reasons outlined above, Applicant respectfully submits that neither Kweon nor Takada disclose, teach or suggest all of the features of the independent claim 4, and dependent claims 18, 19 and 22, which are patentable not only by virtue of their dependency from the respective independent claim 4, but also by the additional limitations they recite.

E. The § 103(a) Rejection of the Prior Art in view of Hashimoto

Regarding claims 20 and 23, first, the references, separately, or in combination, fail to teach, disclose or provide a motivation for being combined.

Hashimoto ("Hashimoto") does not have the same aim as the Prior Art. Hashimoto discloses a compact electronic component and a semiconductor device with an external electrode, i.e., solder ball, within the region of the semiconductor element for external connection and a stress relieving layer. Hashimoto is specifically directed to relieving thermal stress without breaking wire due to the different coefficients of thermal expansion between the semiconductor device chip and a related mounting board. (See Hashimoto at Abstract; Column 1, lines 5-15 and lines 35-50).

Nothing within Hashimoto, which focuses on relieving thermal stress between the semiconductor chip and the mounting board, has anything to do with underfill material for differences in thermal coefficients of expansion as disclosed in the Prior Art. Thus, the Prior Art teaches away from being combined with another invention, such as, Hashimoto.

Therefore, one of ordinary skill in the art would not have combined these references, absent hindsight.

Second, even if combined, the references do not teach or suggest the features of independent claim 20. Specifically, there is no teaching or suggestion of at least one feature, including the second conductive pad includes a second uneven roughness portion in contact with the solder balls.

Hashimoto does not make up for the deficiencies of the Prior Art.

Instead, Figures 2 and 11A of Hashimoto disclose a semiconductor device where the semiconductor device includes a stress relieving layer 36 with a hole 36a. Applicant respectfully submits that the Office Action mischaracterizes Hashimoto because Hashimoto only discloses a solder ball 40 on a plurality of layers (42, 44) in a hole 36a without any uneven roughness not a conductive pad with a roughness. (See Office Action, Pages 7-8, Section 9). In particular, a chromium layer 42 is formed in the hole 36a and a Cu layer 44 is formed on the chromium layer 42. Further, a Cu base 46 is formed on the Cu layer 44 where a solder ball is formed on the Cu layer. Based on this configuration, "stress from the solder ball is transmitted from a stress transmission portion formed from at least a part of the chromium layer, Cu layer and Cu base to the stress relieving layer." Accordingly, this configuration does not teach any printed circuit board with a conductive pad, let alone, a roughness on the conductive pad. Thus, Hashimoto's structure relieves stress on a solder ball through a stress relieving layer without focusing on a connection between a printed circuit board and the chip mounting substrate. (See Column 8, lines 29-56; Column 13, lines 55-62; and Figures 2 and 11A).

In contrast, as discussed above, Applicant's invention disclose includes the second conductive pad which includes a second uneven roughness portion in contact with the solder

balls whereas Hashimoto does not teach any printed circuit board, let alone, with a conductive pad, and certainly no conductive pad with an uneven roughness. Thus, Applicant's configuration increases adhesive strength between the printed circuit board and the solder balls compared to conventional structures using indirect bonding of the components. (See Page 19, lines 1-4; and lines 15-24; Page 20, lines 10-25; and Page 21, lines 18-28; and Figures 5 and 6).

Indeed, Hashimoto does not teach Applicant's structure because Hashimoto is focused on relieving thermal stress between the semiconductor chip and the mounting board. Accordingly, Hashimoto does not disclose, teach or suggest including at least one feature of Applicant's invention, including the second conductive pad includes a second uneven roughness portion in contact with the solder balls. Thus, Applicant's invention provides for greater adhesive strength between the printed circuit board and the solder balls when compared to Hashimoto's structure.

Accordingly, the semiconductor device experiences less internal exfoliation of the components and operates with a high level of reliability. (See Page 3, lines 15-21; See Page 19, lines 1-4; and lines 15-24; Page 20, lines 10-25; and Page 21, lines 18-28; and Figures 5 and 6).

For at least the reasons outlined above, Applicant respectfully submits that neither the Prior Art nor Hashimoto disclose, teach or suggest all of the features of the independent claim 20, and related dependent claim 23.

IV. FORMAL MATTERS AND CONCLUSION

In view of the foregoing, Applicant submits that claims 1- 4 and 16-23, all the claims presently pending in the application, are patentably distinct over the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Attorney's Deposit Account No. 50-0481.

Respectfully Submitted,

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AMENDMENTS TO THE DRAWINGS

In response to the drawing objection, Applicant submits the attached Proposed Submission of Replacement Sheets including Drawing Correction. The Drawing Correction amends Figures 2A-6B to more clearly show the "solder mask" designated as 15 or 46 consistent with the specification on Page 13, lines 20-24 and Page 18, lines 19-21, but currently points to the Cu wiring instead.